AMENDMENTS TO THE CLAIMS:
Please revise the claims, as follows:

1. (Currently amended) A stacked capacitor ~~comprises~~ comprising:

a dielectric layer;

a two-dimensional array of terminal electrodes on at least one of first and second surfaces of said dielectric layer;

first internal electrodes stacked in multi-levels in said dielectric layer, ~~and~~ said first internal electrodes being electrically connected to a power line;

second internal electrodes stacked in multi-levels in said dielectric layer, ~~and~~ said second internal electrodes being electrically connected to a ground line; and

vias in said dielectric layer, ~~so that~~ thereby allowing said terminal electrodes ~~being~~ to be electrically connected through said vias to said first and second internal electrodes,

wherein said two-dimensional array further comprises at least one signal line terminal electrode such that a signal line via connected to said at least one terminal electrode is electrically isolated from said first and second internal electrodes, each said signal line via being surrounded by a low dielectric layer in said dielectric layer, thereby allowing each signal line via to be separated from said dielectric layer, and

wherein all of said first and second internal electrodes are spatially isolated from said low dielectric layers in said dielectric layer.

2. (Original) The stacked capacitor as claimed in claim 1, wherein said two-dimensional array of terminal electrodes are provided on both said first and second surfaces of said dielectric layer.

3. (Original) The stacked capacitor as claimed in claim 1, wherein said two-dimensional array of terminal electrodes comprises alternating alignments of said terminal electrodes connected to said power line and said terminal electrodes connected to said ground line.

4. (Cancel)

5. (Currenty amended) The stacked capacitor as claimed in claim 1, wherein each of said low dielectric layers has a lower dielectric constant than said dielectric layer.

6. (Original) The stacked capacitor as claimed in claim 5, wherein said dielectric constant of said low dielectric layer is at least 40.

7. (Currently amended) The stacked capacitor as claimed in claim ~~5~~ 1, wherein said signal line via comprises a metal containing a glass material.

8. (Currently amended) The stacked capacitor as claimed in claim ~~5~~ 1, wherein said signal line via comprises a metal containing a metal oxide material.

9. (Original) The stacked capacitor as claimed in claim 1, wherein said dielectric layer comprises a perovskite-structured compound.

10. (Currently amended) A semiconductor device comprising:

a printed circuit board;

a semiconductor integrated circuit; and

a stacked capacitor which further comprises:

a dielectric layer;

a two-dimensional array of terminal electrodes on at least one of first and second surfaces of said dielectric layer;

first internal electrodes stacked in multi-levels in said dielectric layer, and said first internal electrodes being electrically connected to a power line;

second internal electrodes stacked in multi-levels in said dielectric layer, and said second internal electrodes being electrically connected to a ground line; and

vias in said dielectric layer, ~~so that~~ thereby allowing said terminal electrodes ~~being~~ to be electrically connected through said vias to said first and second internal electrodes,

wherein said two-dimensional array further comprises at least one signal line terminal electrode such that a signal line via connected to said at least one terminal electrode is electrically isolated from said first and second internal electrodes, each said signal line via being surrounded by a low dielectric layer in said dielectric layer, thereby allowing each signal line via to be separated from said dielectric layer, and

wherein all of said first and second internal electrodes are spatially isolated from said low dielectric layers in said dielectric layer.

11. (Original) The semiconductor device as claimed in claim 10, wherein said stacked capacitor is interposed between said printed circuit board and said semiconductor integrated

circuit.

12. (Original) The semiconductor device as claimed in claim 10, wherein said stacked capacitor is provided on a first surface of said printed circuit board and a second surface of said printed circuit board.

13. (Original) The semiconductor device as claimed in claim 10, wherein said two-dimensional array of terminal electrodes are provided on both said first and second surfaces of said dielectric layer.

14. (Original) The semiconductor device as claimed in claim 10, wherein said two-dimensional array of terminal electrodes comprises alternating alignments of said terminal electrodes connected to said power line and said terminal electrodes connected to said ground line.

15. (Cancel)

16. (Currently amended) The semiconductor device as claimed in claim 10, ~~further comprising a low dielectric layer around said via, and said via is separated from said dielectric layer by said low dielectric layer, and said low dielectric layer~~ wherein each of said low dielectric layers has a lower dielectric constant than said dielectric layer.

17. (Original) The semiconductor device as claimed in claim 16, wherein said dielectric constant of said low dielectric layer is at least 40.

18. (Currently amended) The semiconductor device as claimed in claim ~~16~~ 10, wherein said signal line via comprises a metal containing a glass material.

19. (Currently amended) The semiconductor device as claimed in claim ~~16~~ 10, wherein said signal line via comprises a metal containing a metal oxide material.

20. (Original) The semiconductor device as claimed in claim 10, wherein said dielectric layer comprises a perovskite-structured compound.